IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Inventor(s):	Hisao KOGA et al.	Art Unit 2827
Appln. No.:	10/747,982	Exr. L. Cruz
Filed:	December 31, 2003	
For:	RESIN MOLDED TYPE SEMICONDUCTOR DEVICE AND A METHOD OF MANUFACTURING THE SAME	

PETITION TO MAKE SPECIAL

Assistant Commissioner of Patents
Washington, DC 20231

Sir:

The Applicants respectfully petition that the above-captioned application be granted special status. This application is a continuing application of 09/380,312 filed August 31, 1999. The requirements of MPEP section 708.02(VIII) are complied with as follows:

(1) Please charge the petition fee set forth in 37 CFR 1.17(i) to Deposit Account No. 19-4375.

(2) All pending claims of the present application are believed to be directed to a single invention; if the Office determines that all the claims presented are not obviously directed to a single invention, the Applicants agree to make an election without traverse as a prerequisite to the grant of special status.

(3) A pre-examination search of the invention has been made in the form of search reports in counterpart foreign applications as follows: a Japanese office action dated December 22, 1998, an International Search Report (ISR) dated March 19, 1999, an International Preliminary Examination Report (IPER) dated October 19, 1999, a Notice of Opposition dated March 10, 2000 in a counterpart Japanese application, and a Notice dated August 11, 2000, in a counterpart Japanese application. Under MPEP 708.02, VIII, a search made by a foreign patent office satisfies the search requirement.

(4) One copy each of the prior art deemed most closely related to the subject matter encompassed by the claims is of record in the form of the art cited in the Information Disclosure Statement filed December 31, 2003 (see 37 CFR 1.98(d)).

(5) The following is a detailed discussion of the art cited in the Information Disclosure Statement filed December 31, 2003, and comments pointing out how the instant claimed subject matter is patentably distinguishable thereover.

A. Discussion of Prior Art of Record

The following statements are of record in the parent application. The Tsuchiya (JP 02201946) and Otsuka (JP 04155854)

were the sole references applied in the office actions of the parent application.

The semiconductor device disclosed in Tsuchiya (JP '946) comprises a semiconductor chip 1 mounted on a pad portion (island) 2 of a lead frame, bonding wires 3 which electrically connect the electrodes of the semiconductor chip 1 respectively to the inner side of a lead frame 4, and a resin body 8 which surrounds and seals the peripheral region of chip 1. The peripheral region of chip 1 includes a wire connecting portion on the upper surface of chip 1 and pad portion (island) 2. The outer side of lead frame 4 is disposed on a level with the bottom surface of resin body 8, and pad portion (island) 2 is located in a higher position than the inner side of lead frame 4. Tsuchiya (JP '946) does not discuss the dimensional relationship of chip 1 to island 2. Figure 2(b) of Tsuchiya (JP '946) shows chip 1 smaller in size than island 2.

According to the structure of the semiconductor device of Tsuchiya (JP '946), the sealing resin is not present on the bottom side of chip 1 allowing contact of resin body 8 only to its upper and side surfaces. Consequently, the interactive force of resin body 8 is imposed exclusively to the contacting surfaces of chip 1, resulting in an unstable distribution of the interactive forces. Thus, Tsuchiya (JP '946) will not achieve an effect of sealing

resin present on the bottom surface of chip 1, nor a better balance of interactive forces between the chip surface and the sealing resin, nor a reduction in mechanical damages of the chip due to deformation such as bending.

Otsuka (JP '854) teaches that a bonding pad 4 of a semiconductor chip is electronically connected via bonding wire 5 to grooves 7 formed on the surface of an inner lead 1b.

Koyae (JP '952) discloses arranging leads, which are exposed on the bottom face of a semiconductor chip sealing package, at the sections facing the periphery of the package without projecting to the outside of the periphery. A semiconductor chip 11 is sealed with resin package 13, with leads 21-28 arranged at sections facing periphery 13a of resin package 13 flush with its bottom face 13b and exposed on bottom face 13b without projecting to the outside of periphery 13a. Leads 21-28 have circular through holes 21a-28a and protrusions 21b-28b. Cut-out sections 13a-1-13a-8 are formed where leads 21-28 are arranged, and their through holes 21a-28a are exposed upward. Wires 14 are bonded to chip 11 and at inner edges of leads 21-28. Stage 12 and leads 21-28 are connected to a frame 15 and cut on lines 11-11 after resin sealing. This prevents imperfect soldering caused by a bent lead.

Tsuchiya (JP '946) and Koyae (JP '952) do not teach or suggest, together with any other art of record, the characteristic features of a molded semiconductor device having a flat connecting portion of the metal wire to the inner lead portion disposed between or adjacent to the groove portions and the contact surface of the inner lead portion to the fine metallic wire. According to the disclosure of Koyae (JP '952), grooves 7 are formed on the bonding surface of the inner lead 1b, but this surface is not flat. In Koyae (JP '952), grooves 7 are formed on the surface of inner lead 1b to which bonding wire 5 is connected, but Koyae (JP '952) does not imply that grooves 7 are positioned so that the connecting portion is located between adjacent grooves. Koyae (JP '952) merely discloses a technology where the contact surface of bonding wire 5 to inner lead 1b is increased by contacting bonding wire 5 to the surfaces of a plurality of grooves 7 of the inner lead 1b. The technology is not intended for mitigation of the stress by the presence of two adjacent grooves between which the connecting portion to the thin metal wire is located. This structure does not achieve a result that the stress imposed on the connecting portion of the fine metallic wire located between grooves is distributed evenly to each of the adjacent grooves.

Further, Tsuchiya (JP '946) and Koyae (JP '952) fail to disclose or suggest, alone or together with any other art of record, anything relating to increasing contact area between an inner lead portion and sealing resin for enhancing the anchor effect in the inner lead portion.

Also, Tsuchiya (JP '946) and Otsuka (JP '854) do not disclose or suggest, alone or together with any other art of record, at least a portion of the outer periphery of the semiconductor chip extends outward from the outer periphery of the die pad (see present claims 18 and 26). Tsuchiya (JP '946) and Otsuka (JP '854) do not disclose or suggest sealing resin contacting a bottom face of the semiconductor chip (see present claim 13).

In Tsuchiya (JP '946), the inner lead is unsealed at the bottom surface and wraps around the resin block; thus, it does not have the problem of the lead tending to pull away from the resin block. Therefore, there is no motivation to incorporate into the Tsuchiya (JP '946) device the arrangement of the inner lead portions of Katagiri (JP'042), since the inner lead portions of Katagiri (JP'042) are provided to prevent the leads from being removed from the resin block.

Further, there is no motivation to incorporate into the Tsuchiya (JP '946) device the arrangement of the inner lead

portions of Katagiri (JP'042). In Katagiri (JP'042), sealing resin leaves the entire outer lead portions unsealed, so it has a problem that the outer lead portions tend to pull away from the resin block. But in Tsuchiya (JP '946) Fig. 1(b), sealing resin seals an upper region of the outer lead portions. Thus, Tsuchiya (JP '946) Fig. 1(b) does not have the problem of the outer lead portions tending to pull away from the resin block.

Even if Tsuchiya (JP '946) and Katagiri (JP'042) were combined, the claimed invention achieves unexpected results thereover (see MPEP 716.02(a)). The claimed invention results in the groove portions absorbing a stress acting on the inner lead portions even if the inner lead portions have a single-side molding structure. This stress acting on the inner lead portions occurs only if the inner lead portions have a single-side molding structure. Tsuchiya (JP '946) and Katagiri (JP'042) do not provide for groove portions that absorb stress acting on the inner lead portions even if the inner lead portions have a single-side molding structure. Therefore, the claimed invention has unexpected results.

The JP office action of December 22, 1998 merely states that (1) JP '776 discloses a semiconductor device that is configured so that a pedestal on which an integrated circuit element 5 is placed

is positioned so as to be higher that the bottom face of a mold 7, and a lead portion is exposed from mold 7 through an external bottom face (Fig. 4), (2) JP '856 discloses a semiconductor device in which plural grooves 8 are disposed in the vicinity of a bonding portion 9 of an inner lead portion (Fig. 1), and (3) JP '364 discloses a lead frame in which a wider portion is disposed in a tip end portion of an inner lead.

The JPO stated in the JP Opposition relating to a counterpart application, that JP '776 and JP '380 merely disclose performing an upsetting process on a base portion (JP '776) or a tab (JP '380), which is a semiconductor support portion, in a sealing resin, exposing the lower face and end face of the outer lead portion from the resin, and making the end face be in the same level as a side face of the resin. The JPO stated that the inner lead portions are also subjected to the upsetting process along with the upsetting process of the semiconductor chip portion, and both portions are molded on both sides with resin. The JPO also said that JP '856 and JP '550 merely describe forming groove portions, that is, a plurality of grooves in the upper and lower face, including the tip end portion, of the inner lead of a resin molded type semiconductor device and connecting the wire between the plurality of groove portions, with the grooves being formed exclusively for the purpose

of preventing the intrusion of moisture, and with the inner lead portions being molded on both sides with resin. The JPO said that these references do not suggest a structure in which a plurality of groove portions are formed in the upper face of the tip end portion of each of the inner lead portions and in which the wire is connected between the groove portions. The JPO noted that JP '304 and JP '315 disclose forming a plurality of half etching portions, uneven portions, or grooves in the upper face of the tip end portion of each of the inner leads of a resin molded type semiconductor device, thereby improving the adhesiveness with r4esin and preventing wire cut. The JPO said that JP '132 discloses providing unevenness in the upper face of the peripheral portion of the die pad of a single side molding structure, thereby preventing the interface peeling with resin, but does not suggest absorbing and relaxing stress. The JPO said that JP '364 discloses formation of a widened portion in the tip end portion of each of the inner lead portions.

The IPER said the following:

(1) JP '851 discloses a resin molded type semiconductor device, wherein IC chip 1 and die pad 2 of a lead frame are located almost in the center of sealing resin 5 which seals an outer peripheral region of chip 1, this region including a thin metal

wire region of the upper face of chip 1 and a lower region of die pad 2. Outer portions of leads 3 are arranged in a bottom face region of resin 5. Die pad 2 is located at a position higher than the inner portions of leads 3. Wires 4 connect terminals of an upper face of chip 1 to inner portions of leads 3 of the lead frame. External lead 3, having the same plane surface as the bottom face of sealed resin 5, is formed and exposed. According to the reference, the purpose of this structure is to prevent the generation of cracks on the sealed resin and the infiltration of moisture into chip 1, thereby improving the damp-proof property of the semiconductor device.

(2) JP '455 discloses a resin molded type semiconductor device, wherein chip 4 is mounted on a die pad of a lead frame 1, thin metal wires 5 electrically connect terminals of an upper face of chip 4 to inner lead portions of lead frame 1, sealing resin 6 seals an outer peripheral region of chip 4, this region including a thin metal wire region of the upper face of chip 4, and outer lead portions are arranged in a bottom face region of the sealing resin 6 and formed to be continuous to respective inner lead portions. A groove portion 2 is formed in a surface of each of the inner lead portions. The object is to improve manufacture efficiency and size accuracy. Excess adhesive 3 is absorbed by

groove 2 so as not to be exposed to the terminal surface of lead frame 1 and not to flow out to the junction parts of metal wires 5.

(3) JP '473 discloses using the rear sections of inner leads connected to internal wiring as external electrodes at the time of directly mounting the semiconductor device. Chip 1 is placed on die pad 2 and connected to inner leads 6 of a lead frame through bonding wires 3. The rear parts of inner leads 6 become external electrodes 8. The upper part is sealed with a resin. Chip 1 is also electrically connected to the leads through bumps 4. Therefore, the size and thickness of the semiconductor device can be reduced.

(4) JP '456 discloses a resin molded type semiconductor device, wherein chip 16 is mounted on a die pad 11 of a lead frame, thin metal wires 17 electrically connect terminals of an upper face of chip 16 to inner lead portions 12 of the lead frame, sealing resin 18 seals an outer peripheral region of chip 16, this region including a thin metal wire region of the upper face of chip 16, and outer lead portions 12 are arranged in a bottom face region of sealing resin 18 and formed to be continuous to respective inner lead portions 12. A widened portion is formed in each of the inner portions of leads 12. A stair part 15 provided on a lead frame 20 is also covered with sealing resin 18, whereby a

reinforcing bar 19 exposed to an end surface of sealing resin 18 is also of the same projection type so as to have very strong structure against coming-off even to external force and thermal strain.

All of the US patents of record were cited in an office action in the parent application dated December 20, 2001, but were never applied as a basis for rejection. The Applicants agree with the position taken in the office actions in the parent application that such references do not provide any basis for rejection of the present invention.

B. Discussion of How the Claimed Invention Patentably Distinguishes over the References of Record

The prior art of record fails to teach or suggest at least the following combination of features of the independent claims.

Independent claim 11 recites that at least one groove portion is formed in a surface of each of the inner lead portions, and a connecting portion of each of the thin metal wires is coupled to a respective inner lead portion at a flat surface region of the respective inner lead portion adjacent the at least one groove portion.

Independent claim 13 recites that the sealing resin contacts a bottom face of the semiconductor chip and that outer lead portions are arranged in a bottom face region of the sealing resin

and are formed to be continuous to respective inner lead portions. The prior art of record does not disclose or suggest such subject matter.

Independent claim 14 recites that thin metal wires electrically connect terminals of the semiconductor chip to the inner lead portions at a position not on top of the groove portion; and a sealing resin seals the groove portion, an outer peripheral region of the semiconductor chip and an entire upper region of the inner lead portions, with the outer peripheral region including a region of the thin metal wires, and the sealing resin leaves an entire bottom surface of the inner lead portions unsealed.

Independent claim 22 recites thin metal wires which electrically connect terminals of the semiconductor chip to the leads at a position not on top of the groove portion; and a sealing resin which seals the groove portion, the thin metal wires, the semiconductor chip and an upper region of the leads, wherein the sealing resin leaves an entire bottom surface of the leads unsealed.

In JP'946, the inner lead is unsealed at the bottom surface and wraps around the resin block; thus, it does not have the problem of the lead tending to pull away from the resin block. Therefore, there is no motivation to incorporate into the JP'946

device the arrangement of the inner lead portions of JP'042, since the inner lead portions of JP'042 are provided to prevent the leads from being removed from the resin block.

Also, there is no motivation to incorporate into the JP'946 device the arrangement of the inner lead portions of JP'042 for further reasons that in JP'042, sealing resin leaves the entire outer lead portions unsealed, so it has a problem that the outer lead portions tend to pull away from the resin block. But in JP'946 Fig. 1(b), sealing resin seals an upper region of the outer lead portions. Thus, JP'946 Fig. 1(b) does not have the problem of the outer lead portions tending to pull away from the resin block.

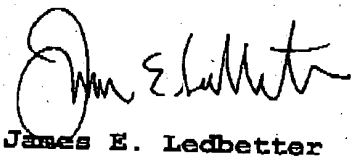
Even if JP'851 and JP'042 were combined, the claimed invention achieves unexpected results thereover (see MPEP 716.02(a)). The claimed invention results in the groove portions absorbing a stress acting on the inner lead portions even if the inner lead portions have a single-side molding structure. This stress acting on the inner lead portions occurs only if the inner lead portions have a single-side molding structure. JP'946 and JP'042 do not provide for groove portions that absorb stress acting on the inner lead portions even if the inner lead portions have a single-side molding structure. Therefore, the claimed invention has unexpected results.

For at least the above reasons, all of the pending independent claims, and the claims dependent therefrom, patentably distinguish over the individual or combined teachings of the prior art of record.

Accordingly, in light of the foregoing discussion pointing out how the claimed invention distinguishes over the cited references, the Applicants respectfully submit that the inventions of all the presently pending claims are not anticipated by these references and would not have been obvious over any combination thereof.

Grant of special status in accordance with this petition is respectfully requested.

Respectfully submitted,



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